UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,550	11/26/2003	Tokio Miyasita	031948-4	6273

22204 7590 06/09/2004

NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASINGTON, DC 20004-2128

EXAMINER	
NGUYEN, JOHN B	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,550	MIYASITA ET AL.	
	Examiner	Art Unit	
	John B Nguyen	2819	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3 and 17 is/are rejected.

7)☒ Claim(s) 2 and 4-16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11/26/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/26/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Information Disclosure Statement

2. Information Disclosure Statement (IDS) form PTO-1449 filed on 11/26/03 has been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,3 are rejected under 35 U.S.C. 102(e) as being anticipated by Shigemasa et al. (Pub. No. US 2003/0123567 A1).

4. Regarding to claim 1, Shigemasa et al disclose a demodulating circuit (Fig. 2) for

demodulating a pulse signal (page 3, para. 0043) including runs of identical '1' or '0' (page 3, para. 0043) symbols, comprising: a differentiating circuit (33) for detecting voltage changes at rising and falling transitions of the pulse signal (page 3, para. 0042, 0043) and outputting a differentiated signal responsive to the voltage changes (page 3, para 0042, 0043); and a hysteresis comparator (34) for comparing the differentiated signal (VA) with a first reference voltage (VB) according to a predetermined upper threshold voltage higher than the first reference voltage (page 3, para. 0042) and a predetermined lower threshold voltage lower than the first reference voltage (page 3, para. 0042), thereby generating a demodulated signal that maintains first logic level when the differentiated signal is above the upper threshold voltage (page 3, para. 0042), maintains second logic level when the differentiated signal is below the lower threshold level (page 3, para. 0042), and maintains an existing one of the first and second logic levels without changing when the differentiated voltage is between the upper threshold voltage and the lower threshold voltage (hysteresis comparator 34).

5. Regarding to claim 3, the demodulating circuit of claim 1, wherein: the hysteresis comparator (34) comprises a comparator element having an inverting input terminal (-) for receiving the differentiated signal (VA), a non-inverting input terminal (+) for receiving the first reference voltage (VB) used for voltage comparison, and an output terminal (output from COMP1) for output of the demodulated signal; a first resistance (R3) element coupling the output terminal of the comparator element to the non-inverting input terminal of the comparator element (R3 connected between output

COMP1 to + terminal), and a second resistance (R2) element coupling the first reference voltage (VB) to the non-inverting input terminal (+) of the comparator element; and the differentiating circuit (33) comprises a differentiating capacitor (C1) coupling the pulse signal (c) to the inverting input terminal (-) of the comparator element, and a third resistance element (R1) coupling the first reference voltage (VB) to the inverting input terminal (-) of the comparator element for charging and discharging the differentiating capacitor.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemasa et al. (Pub. No. US 2003/0123567 A1) in view of Crawford (U.S.Patent No. 6,496,549 B1).

Regarding to claim 17, Shigemasa et al. disclose all limitations but fails to disclose an optical receiving circuit using the demodulation circuit to receive a burst optical signal used in optical comunication. However, Crawford discloses an optical receiving circuit that using the demodulation circuit (Column 1, lines 12-16) to receive a bust optical signal (column 1, lines 12-16). Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to combine the demodulation circuit of Shigemasa to the system of Crawford to provide the better communication system.

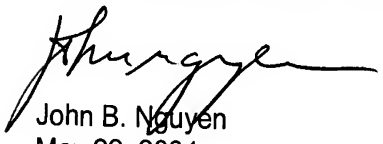
ALLOWABLE SUBJECT MATTERS

8. Claims 2, 4-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See enclosed Form PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B Nguyen whose telephone number (571) 272-1808. The examiner can normally be reached on 8AM-4: 30 PM M-F.



John B. Nguyen
May 22, 2004